Lecture 6: Multistage Logic Networks

- Multistage Logic Networks

- Reading: Ch. 4

Multistage Logic Networks

- *Path Logical Effort*

![Diagram of multistage logic network with gates and logical effort values.](image-url)
Multistage Logic Networks

- *Path Electrical Effort*

- Logical effort generalizes to multistage networks
Paths that Branch

• Consider paths that branch:

\[
\begin{align*}
G &= \\
H &= \\
GH &= \\
h_1 &= \\
h_2 &= \\
F &= 
\end{align*}
\]

Branching Effort

• Introduce branching effort

• The branching effort is:
Paths that Branch

- Consider paths that branch:

\[ G = \]
\[ H = \]
\[ B = \]
\[ GBH = \]
\[ h_1 = \]
\[ h_2 = \]
\[ F = \]

Path Effort

- *Path Logical Effort*

- *Path Electrical Effort*

- *Branching Effort*

- *Path Effort*

- *Note:*
Multistage Delays

- Path Effort Delay
- Path Parasitic Delay
- Path Delay

Designing Fast Circuits

\[ D = \sum d_i = D_F + P \]

- Delay is smallest when each stage bears same effort

- Thus minimum delay of N stage path is

- This is a key result of logical effort
Example: 3-stage path

Recall FO4 Inverter

- Estimate the delay of a fanout-of-4 (FO4) inverter
Gate Sizes

• How wide should the gates be for least delay?

• Check work by verifying input cap spec is met.

Example: 3-stage path

• Select gate sizes x and y for least delay from A to B
Example: 3-stage path

- Work backward for sizes
  \[ y = \]
  \[ x = \]
  \[ \]

Check Results

- NAND2 Delay: \[ d_1 = \]
- NAND3 Delay: \[ d_2 = \]
- NOR2 Delay: \[ d_3 = \]
- \[ D = \]
Discussion