EEL 5322  
VLSI Circuits and Technology  
Fall 2005

Instructor  
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Office Hours  
MWF 3:00-3:50

Time and Location  
NEB 202  
MWF 1:55-2:45 (7)

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Required Textbooks  
Richard C. Jaeger, "Introduction to Microelectronic Fabrication,"  
Second Edition, Modular Series on Solid State Devices, Volume 5,  


Course Goals  
-To develop proficiency in analyses, design and implementation of CMOS circuits.  
-To provide a brief overview of microelectronic fabrication theory.  
The majority of the course will be devoted to developing a basic understanding of CMOS integrated circuit design.

Computer/software req.  
Workstations with CADENCE Design system.

Grading policy  
This is a tentative grading policy.

Homework: 15% (8-10 HWs)  
Project: 25%  
Midterms: 30% (two midterms)  
Final 30%
### Academic Honesty
All students admitted to the University of Florida have signed a statement of academic honesty committing themselves to be honest in all academic work and understanding that failure to comply with this commitment will result in disciplinary action.

This statement is a reminder to uphold your obligation as a student at the University of Florida and to be honest in all work submitted and exams taken in this class and all others.

### Student with disability
Students requesting classroom accommodation must first register with the Dean of Students Office. The Dean of Students Office will provide documentation to the student who must then provide documentation to the instructor when requesting accommodation.

### Other
No make-up exam/homework unless there is a very good reason. This will be handled on case by case basis. Class attendance is required.
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<tr>
<th>Wk</th>
<th>Date</th>
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<th>Topic</th>
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<tbody>
<tr>
<td>Aug 1</td>
<td>W 24</td>
<td>1</td>
<td>Introduction</td>
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</tbody>
</table>
| F 26 | 2 | Integrated circuits  
Ion Implantation |
| 2 M 29* | 3 | Ion Implantation |
| W 31* | 4 | Diffusion |
| Sept F 2 | 5 | Diffusion |
| 3 M (5) | Labor Day: No class |
| W 7 | 6 | Oxidation |
| F 9 | 7 | Oxidation |
| 4 M 12 | 8 | Film Deposition |
| W 14 | 9 | Etching |
| F 16 | 10 | Photolithography |
| 5 M 19 | 11 | Yield |
| W 21 | 12 | Critical dimensions and alignment |
| F 23 | 13 | CMOS-twin well process flow |
| 6 M 26 | 14 | Design rules |
| W 28 | 15 | MOS device:  
MOS regions, subthreshold, 2nd order effects |
| F 30 | 16 | MOS device:  
MOS capacitance, unified analytical model |
| Oct 7 M 3 | Exam I |
| W 5 | 17 | MOS device:  
latch-up and isolation |
| F (7) | Home Coming: No class |
| 8 M 10 | 18 | CMOS Inverter:  
Inverter characteristics, trip point analysis |
| W 12 | 19 | CMOS Inverter:  
Noise margin and gain |
| F 14 | 20 | CMOS Inverter:  
Propagation delay, velocity sat. and long channel models, finite rise time |
| 9 M 17 | 21 | CMOS Inverter:  
Capacitance, Power dissipation |
| W 19 | 22 | Interconnect:  
Resistance and capacitance |
| F 21 | 23 | Interconnect:  
Elmore delay |
| 10 M 24 | 24 | Interconnect:  
Transistor sizing, repeater insertion |
| W 26 | 25 | Cadence Tutorial |
| F 28 | 26 | Combinational logic:  
Mapping Boolean functions |
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<thead>
<tr>
<th>Date</th>
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</thead>
<tbody>
<tr>
<td>Nov</td>
<td>W</td>
<td>2</td>
<td>28</td>
<td>Combinational logic: CMOS static gates</td>
</tr>
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<td>29</td>
<td>Combinational logic Dynamic circuits</td>
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<td>12</td>
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<td>Exam II</td>
<td></td>
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<td>W</td>
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<td>31</td>
<td>Combinational logic: Process variations, Process independent design</td>
</tr>
<tr>
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<td>F</td>
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<td>Veterans Day: No class</td>
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<td>Project Assignment</td>
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<td></td>
<td>W</td>
<td>16</td>
<td>Sequential Logics: Timing basics, Latches vs. Registers</td>
<td></td>
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<td></td>
<td>F</td>
<td>18</td>
<td>Sequential Logics: Setup/Hold time, design issues</td>
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<td>14</td>
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<td>21</td>
<td>Sequential Logics: Design considerations</td>
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<td>W</td>
<td>23</td>
<td>Sequential Logics: Types of FF</td>
<td></td>
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<td>(25)</td>
<td>Thanksgiving: No class</td>
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<td>Dec</td>
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<td>28</td>
<td>Memory -types</td>
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<td>W</td>
<td>30</td>
<td>Memory - architecture</td>
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<td></td>
<td>F</td>
<td>2</td>
<td>Memory – core, SRAM cells</td>
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<tr>
<td>16</td>
<td>M</td>
<td>5</td>
<td>Review</td>
<td></td>
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<td></td>
<td>W</td>
<td>7</td>
<td>Classes End: Final Project Due</td>
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<td>12</td>
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<td>13</td>
<td>Final Exam 3:00PM-5:00PM NEB 202</td>
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* Video-taped
Tentative schedule
**Topic 0 – Introduction (1)**
Introduction
Integrated circuits

**Topic 1 – Microelectronic Fabrication (9)**
Ion implantation (ion implanter benefits, ion ranges, selective implantation, damage and annealing, channeling)
Diffusion (diffusion process, fick’s law, diffusion coefficient, constant/limited profiles, two-step diffusion, junction formation)
Oxidation (oxidation reactions and process, growth rate, consumption of Si)
Film deposition (chemical vapor deposition, types of CVD, physical vapor deposition, chemical mechanical polishing)
Etching (rate, anisotropy, bias, selectivity, variations)
Photolithography

**Topic 2 – Process integration and design rules (4)**
Yield
Critical dimension and Alignment
CMOS-twin well process flow
Design rules

**Topic 3 – MOS device (3.5)**
MOS regions of operations
Sub-threshold region
2nd order effects (Body effect, CLM, narrow width, mobility variation, S/D resistance, DIBL)
MOS Capacitance (regions)
MOS Analytical Models (Unified model)
SPICE parameters
Latch-up and isolation

**Topic 4 – CMOS Inverter (4)**
MOS inverter characteristics
Inverter trip point analysis (short and long channel assumptions)
Inverter noise margin and gain
Inverter – Dynamic behavior
Propagation delay
Velocity saturated, long channel and general form delay models
Finite input rise time
Inverter output capacitance
Power dissipation (static, subthreshold, dynamic, short-circuit)

**Topic 5 – Wire (3.5)**
Resistance (sheet resistance, resistance values)
Capacitance (formulas, co-linear capacitance)
Elmore delay
Transistor sizing (buffers, optimal number of stages)
Repeater Insertion
**Topic 6 – Combinational logic (4.5)**

Static CMOS
Mapping Boolean functions into CMOS networks
Design of CMOS networks
Dual graphs
Stick diagrams
Common static CMOS gates
Switching and data dependent delay (design considerations)
Transmission gates (TG) – operation, TG resistance
Logic styles - TG, Ratioed, Pseudo NMOS, Cascode Voltage Switch Logic (CVSL), Differential Cascode Voltage Switch Logic (DCVSL), Pass transistor, Complementary pass transistor (CPL)
Dynamic CMOS – issues in dynamic design, cascading dynamic gates
Domino logic – n-block, p-block, np-domino (zipper), NORA – no race, phi-section, Pipelined structures
Modeling process variation, Process independent design

**Topic 7 – Sequential logic circuits (5)**

Timing conventions
Clock skew
Latches vs. Registers
Hard and soft edge properties
Master-slave registers
Delay vs. setup/hold time
Metastability
CMOS register design – design consideration
Types of registers – master-slave vs. pulsed triggered
Master-slave - Power PC, Modified C²MOS MS latches, Single Transistor clocked latches (STC)
Pulsed Triggered – Hybrid latch FF, Semi-dynamic FF, Sense amplifier based FF, Modified SAFF.
Low swing FF

**Topic 8 – Memory (3)**

Memory types
Architecture
Memory core - SRAM cell