Lecture 11: Inversion Coefficient

- Notes from
  Tradeoffs and Optimization in Analog CMOS Design
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  University of North Carolina at Charlotte, USA

- Review of notes from Dr. Fox

- Example from
  A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications
  Reid R. Simmons, Jonathan D.F.C. and Cameron Clapson, Victor VanRoey, 2007

Bipolar collector current and transconductance

- The bipolar transistor collector current, base–emitter voltage relationship is given by
  \[ I_C = I_S e^{\frac{v_{BE}}{U_T}} \]

- Bipolar Transconductance
  \[ g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{U_T} \]
  \[ g_m = \left( \frac{g_m}{I_C} \right) \cdot I_C \]

- Bipolar transistor transconductance efficiency
  \[ \frac{g_m}{I_C} = \frac{I_C}{U_T} = \frac{1}{U_T} \]

For a thermal voltage UT = 25.9mV at room temperature (300K or 27°C), bipolar transistor transconductance efficiency is 38.6V or 38.6µS/µA. This means a transconductance of 38.6µS or 38.6mS is produced for a collector bias current of 1A or 1mA, respectively, found by multiplying the transconductance efficiency by the collector bias current.
MOS Drain Current and Transconductance

**In Weak Inversion**

In weak inversion, the drain-source saturation voltage is frequently taken as $V_{DS_{sat}} = V_{GS} - V_T$, while $V_{DS_{sat}} = (V_{GS} - V_T)/n$ may be a better choice since body effect along the channel raises the local threshold voltage and lowers the drain-source voltage required for inversion charge pinch-off.

Transconductance efficiency in strong inversion is then given by

$$\frac{g_m}{I_D} = \frac{2}{\sqrt{\frac{2 I_D}{V_{G_S} - V_T}}} = \frac{2}{\sqrt{\frac{2 I_D}{V_{G_S} - V_T}}}$$

For a thermal voltage $U_T = 25.9$mV at room temperature and substrate factor $n = 1.5$, MOS weak inversion transconductance efficiency is 25.7uS/uA, which is approximately 67% of the bipolar transistor transconductance efficiency of 38.6uS/uA where $n$, again, is effectively unity.

In weak inversion, $n$ is related to the capacitive voltage division between the gate voltage and silicon surface potential resulting from the gate-oxide, depletion, and interface state capacitances. In weak inversion, $n$ is expressed by

$$n = \frac{C_{GS} + C_{GD} + C_{DS}}{\frac{C_{GD}}{C_{ox}} + \frac{C_{DS}}{C_{ox}} + \frac{C_{GS}}{C_{ox}}}$$

The required increase in gate–source voltage for a factor-of-10 increase in drain current is given by the subthreshold swing

$$S = \ln(10) n U_T = 2.303 \cdot n U_T \text{ (mV/decade)}$$

The weak inversion swing is approximately 90 mV/decade for bulk CMOS processes at room temperature, assuming $n = 1.5$ and $U_T = 25.9$mV.
In Moderate Inversion and All Regions of Operation

- Unified expressions for drain current
  - More complex expression include velocity saturation, DIBL, CLM effects

<table>
<thead>
<tr>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D(WI) = 2\pi \mu_C C_{ox} U_{DS} \left( \frac{W}{L} \right) \left( \frac{V_{GS} - V_T}{e^{\frac{V_{DS}}{V_T}} - 1} \right)$</td>
</tr>
<tr>
<td>$I_D(SI) = \frac{1}{2} \left( \frac{2\mu_C C_{ox}}{e} \right) \left( \frac{W}{L} \right) (V_{GS} - V_T)^2$</td>
</tr>
<tr>
<td>$I_D(WI-SI) = 2\pi \mu_C C_{ox} U_{DS} \left( \frac{W}{L} \right) \left( \ln \left( 1 + e^{\frac{V_{GS} - V_T}{2V_T}} \right) \right)^2$</td>
</tr>
</tbody>
</table>

Designing with Inversion Coefficient (IC)

- Bias point of the MOS transistor can be quantified by
  - Gate overdrive $V_{GS} - V_T$
  - Transconductance current ratio, $g_{m}/I_D$
  - Or the inversion coefficient (IC)

Inversion Coefficient (IC) is a normalized measure of MOS drain current that numerically describes the level of channel inversion.
Inversion Coefficient (IC)

Equating the weak-inversion transconductance, with the strong-inversion transconductance, gives

\[
\frac{g_m}{I_D} = \frac{I_D}{nU_T} = g_m = \sqrt{2L \left( \frac{\mu C_{ox}}{n} \right) \left( \frac{W}{L} \right)}
\]

Solving for the drain current \( I_D = \text{ID (moderate)} \) that gives equal weak- and strong-inversion transconductance gives

\[
I_D = \frac{2n\mu C_{ox} U_T^2}{W/L}
\]

This is the drain current for a device operating in the center of moderate inversion where the predicted weak- and strong-inversion transconductances are equal.

Define IC as the ratio of \( I_D \) to \( I_D \) in Moderate Inversion

\[
IC = \frac{I_D}{I_D (\text{M.I.})} = \frac{I_D}{2n\mu C_{ox} U_T^2} = \frac{I_D}{I_D (W/L)}
\]

\( I_D \) is the technology current

\[
I_D = 2n\mu C_{ox} U_T^2
\]

Relationship between transconductance efficiency and IC

Differentiating the drain current with respect to the gate–source voltage followed by dividing by the drain current

\[
\frac{g_m}{I_D} = \frac{1 - e^{-\sqrt{IC}}}{nU_T \sqrt{IC}}
\]

A more accurate expression

\[
\frac{g_m}{I_D} = \frac{1}{nU_T \left( \sqrt{IC} + 0.5 \sqrt{IC} + 1 \right)}
\]

And simple expression

\[
\frac{g_m}{I_D} = \frac{1}{nU_T \left( \sqrt{IC} + 0.25 + 0.5 \right)}
\]
$V_{\text{EFF}}$ and IC

$V_{\text{EFF}}$ from weak through strong inversion can be derived from the continuous drain current expression.

$$I_D = 2\pi \mu_0 C_{\text{ox}} U_T^2 \left( \frac{W}{L} \right) \ln \left( 1 + \frac{V_{GS} - V_T}{2nU_T} \right)$$

Solving for $V_{\text{EFF}}$ in terms of the inversion coefficient requires expressing drain current in terms of the inversion coefficient.

$$I_D = 2\pi \mu_0 C_{\text{ox}} U_T^2 \left( \frac{W}{L} \right) \cdot IC$$

Substituting the drain current

$$IC = \left[ \ln \left( 1 + \frac{V_{GS} - V_T}{2nU_T} \right) \right]^2$$

Solving for $V_{\text{EFF}}$ gives

$$V_{\text{EFF}} = 2nU_T \ln (e^{\sqrt{IC}} - 1)$$

Inversion Coefficient (IC)

- For analog design useful to define $g_m/I$ valid over all regions of operation using EKV model [Enz, et al., Analog Integrat. Circuits Signal Process., 1995]:

$$\frac{g_m}{I_D} = \frac{1 - e^{-\sqrt{IC}}}{nU_T \sqrt{IC}} \approx \frac{1}{nU_T} \frac{2}{1 + \sqrt{1 + 4 \cdot IC}}$$

$$V_{\text{EFF}} = V_{GS} - V_T = 2 \cdot n \cdot U_T \ln (e^{\sqrt{IC}} - 1)$$
Typical Drain Current Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>nMOS</th>
<th>pMOS</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$</td>
<td>Gate-oxide thickness</td>
<td>13.5</td>
<td>13.5</td>
<td>nm</td>
</tr>
<tr>
<td></td>
<td>0.5 μm, PD SOI</td>
<td>8</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>4.1</td>
<td>4.1</td>
<td></td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>Gate-oxide capacitance</td>
<td>2.56</td>
<td>2.56</td>
<td>$\text{fF}/\mu\text{m}^2$</td>
</tr>
<tr>
<td></td>
<td>0.5 μm, PD SOI</td>
<td>4.31</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>8.41</td>
<td>8.41</td>
<td></td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>Mobility (low field)</td>
<td>438</td>
<td>152</td>
<td>$\text{cm}^2/\text{V} \cdot \text{s}$</td>
</tr>
<tr>
<td></td>
<td>0.5 μm, PD SOI</td>
<td>372</td>
<td>135</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>422</td>
<td>80.2</td>
<td></td>
</tr>
<tr>
<td>$k_t = \mu_0 C_{ox}$</td>
<td>Transconductance factor (low field)</td>
<td>112</td>
<td>59</td>
<td>$\mu\text{A}/\sqrt{\text{V}}$</td>
</tr>
<tr>
<td></td>
<td>0.5 μm, PD SOI</td>
<td>160</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>355</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>$n_0$</td>
<td>Substrate factor (average moderate inversion value)</td>
<td>1.4</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5 μm</td>
<td>1.4</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>1.35</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td>$I_d = 2n_0\mu_0 C_{ox} U_0^{1/2}$</td>
<td>Technology current</td>
<td>0.21</td>
<td>0.07</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td>0.5 μm, PD SOI</td>
<td>0.50</td>
<td>0.105</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.18 μm</td>
<td>0.64</td>
<td>0.135</td>
<td></td>
</tr>
</tbody>
</table>

Shape Factor and Gate Size

- Recall $IC = \frac{I_d}{I_d(\text{M.F.})} = \frac{I_d}{2n_0\mu_0 C_{ox} U_0^{1/2}} = \frac{I_d}{I_d\left(\frac{W}{L}\right)}$

- Two ways to change IC
  - Through drain current (ID) or
  - Gate size W/L, or the shape factor (S)

\[
S = \frac{W}{L} = \left(\frac{1}{IC}\right)\left(\frac{I_d}{I_d}\right) - \left(\frac{1}{10}\right)\left(\frac{100 \mu\text{A}}{0.64103 \mu\text{A}}\right) = 15.6
\]

the technology current of $I_d = 2n_0\mu_0 C_{ox} U_0^{1/2} = 0.64103 \mu\text{A}$

Or, W derived from fixed ID and L

\[
W = S \cdot L = \left(\frac{1}{IC}\right)\left(\frac{I_d}{I_d}\right) - \left(\frac{0.18 \mu\text{m}}{10}\right)\left(\frac{100 \mu\text{A}}{0.64103 \mu\text{A}}\right) = 2.8 \mu\text{m}
\]
MOSFET Noise

- Dominant noise sources for MOSFET
  - Thermal noise and
  - Flicker noise due to carrier trapping and de-trapping from SiO₂ interface

\[
\begin{align*}
V_0(f) &= \frac{K_F}{C_{ox}WL} \cdot f^{-\alpha} \\
I_0(f) &= 4kT \cdot n\Gamma g_m \\
V_n^2(f) &= \frac{K_F}{C_{ox}WL} \cdot f^{-\alpha} + 4kT \cdot n\Gamma g_m \\
\end{align*}
\]
- Gate referred noise
- \( K_F \) flicker noise factor and \( \alpha \) is the frequency exponent
- \( \Gamma \) is 0.5 in W.I. and 2/3 in S.I.
- \( n \) is the substrate factor

Gate Referred Thermal Noise

- Gate referred thermal noise for MOSFET

\[
V_n^2(f) = 4kT \cdot n\Gamma g_m
\]

- Input referred noise for fixed \( I_D \) increases with increasing inversion level
  - saturation thermal noise factor \( \Gamma \) increases
    - 1/2 in W.I. and 2/3 in S.I.
  - \( g_m \) decreases in strong inversion as \( I_C \) increases
- Flicker noise coefficient also increases in strong inversion

Note that \( V_n^2 \) decreases as \( I_D \) increases
(even as \( I_C \) increases)
Amplifier Design Example with IC

Recall Noise Analysis

### Transfer Functions, Referred to Input

\[ \Delta V_{\text{out}} = \sum_{k=1}^{N} G_{\text{in}k} \Delta V_{\text{in}k} \]

\[ \Delta V_{\text{in}} = \frac{\Delta V_{\text{out}}}{G_{\text{in}}} \]

**Input to Output**

\[ (\Delta V_{\text{in}})^2 - (\Delta V_{\text{out}})^2 = G_{\text{in}}^2 \left[ 1 + \sum_{k=1}^{N} \left( \frac{2G_{\text{in}k} \Delta V_{\text{in}k}}{G_{\text{in}}} \right)^2 \right] \]

5 steps to reduce input referred effects of variations:
- Minimize \( \Delta V_{\text{in}} \) (input variation)
- Minimize \( G_{\text{in}} \) (input stage transconductance)
- Reduce \( G_{\text{in}} \) of loads
- Minimize \( \Delta V_{\text{load}} \) of loads
Input Referred Noise

Analysis of this circuit reveals the input-referred thermal noise power to be

$$\sigma_{n,\text{thermal}}^2 = \frac{4kT}{g_{m1}} \left( \frac{1}{2} + \frac{g_{m2} + g_{m3}}{g_{m3}} \right) \Delta f.$$  \hspace{1cm} (4)

where \(\Delta f\) is the phase margin. As \(M_1\) and \(M_3\) are made longer, the OTA input capacitance \(C_{in}\) increases. The input-referred noise of the hoiosmulator can be related to the OTA input-referred noise by

$$\frac{\sigma_{n,\text{nor}}^2}{\sigma_{n,\text{in}}^2} = \left( \frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 \frac{1}{\nu_{n1}}.$$  \hspace{1cm} (5)

where \(C_2\) and \(C_3\) are the feedback network capacitors shown in Fig. 1. Since \(C_{in}\) contributes to a capacitive divider that attenuates the input signal, any increase in \(C_{in}\) increases the input-referred noise of the overall circuit [26]. An optimum gate area

<table>
<thead>
<tr>
<th>Devices</th>
<th>(W/L) ((\mu m))</th>
<th>(I_{D1} (\mu A))</th>
<th>Inversion Coefficient</th>
<th>(g_{m1}/I_{D1} (V^{-1}))</th>
<th>(V_{EFP} = V_{CE} - V_{F1} (V))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1)</td>
<td>400/0.4</td>
<td>1.0</td>
<td>0.43</td>
<td>20.6</td>
<td>-0.076</td>
</tr>
<tr>
<td>(M_2)</td>
<td>12.0/44.8</td>
<td>4.0</td>
<td>71.0</td>
<td>10.5</td>
<td>-0.070</td>
</tr>
<tr>
<td>(M_3)</td>
<td>6.4/12.8</td>
<td>4.0</td>
<td>171.1</td>
<td>2.9</td>
<td>-0.096</td>
</tr>
<tr>
<td>(M_4)</td>
<td>20.0/2.0</td>
<td>8.0</td>
<td>71.1</td>
<td>2.9</td>
<td>-0.096</td>
</tr>
<tr>
<td>(M_{ref})</td>
<td>12.0/3.2</td>
<td>4.0</td>
<td>7.8</td>
<td>8.1</td>
<td>-0.290</td>
</tr>
<tr>
<td>(M_{ref})</td>
<td>6.4/0.2</td>
<td>4.0</td>
<td>45</td>
<td>3.9</td>
<td>-0.481</td>
</tr>
</tbody>
</table>

Noise Efficiency Factor

Since we are interested in minimizing noise within a strict power budget, we must consider the tradeoff between power and noise. The noise efficiency factor (NEF) introduced in [7] quantifies this tradeoff:

$$\text{NEF} = \frac{V_{EFP}}{V_{EFP} + V_{in}}$$  \hspace{1cm} (6)

where \(V_{EFP}\) is the input-referred max noise voltage, \(I_{D1}\) is the total amplifier supply current, and \(BW\) is the amplifier bandwidth in hertz. A high-performance single bipolar transistor (with no \(1/f\) noise) has an NEF of one; all practical circuits have higher values.

Substituting the expression for amplifier thermal noise (4) integrated across the bandwidth \(BW\) into (6) and assuming \(g_{m2} \ll g_{m1}\), we find

$$\text{NEF} = \sqrt{\frac{4I_{D1}}{3U_T^2}} \sqrt{\frac{16}{g_{m1}}}.$$  \hspace{1cm} (7)

where \(I_{D1}\) is the drain current through \(M_1\), which is 1/4 of the total amplifier supply current. From this expression, it is clear that if we wish to minimize the NEF, we must maximize the transconductance \(g_{m2}/I_{D1}\) of the input devices \(M_1\) and \(M_2\). In weak inversion, \(g_{m2}/I_{D1}\) reaches its maximum value of \(n/U_T\), so we make \(W/L\) very large to approach subthreshold operation with microamp current levels. Using a more accurate model for thermal noise valid in weak inversion [21] yields

$$\text{NEF} = \sqrt{\frac{4}{g_{m1}^2}} \left( \frac{I_{D1}}{g_{m1}} \right).$$  \hspace{1cm} (8)

In weak inversion, the expression for NEF reduces to

$$\text{NEF} = \sqrt{\frac{4}{n^2}} \cong 2.0.$$  \hspace{1cm} (9)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 6, DECEMBER 1987
Supply current versus normalized noise